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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,048	10/12/2001	Stephen Clarke	S1022/8767	1792

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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
KENDALL, CHUCK O	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,048	CLARKE, STEPHEN	
	Examiner	Art Unit	
	Chuck Kendall	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed 12/28/04.

2. Claims 1 – 11 are pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Callahan, II USPN 6,321,379 B1.

Regarding claim 1, Callahan anticipates a method of compiling a computer program from a sequence of computer instructions including a plurality of first, set branch, instructions which each identify a target address for a branch and a plurality of associated second, effect branch instructions which each implement a branch to a target address, the method comprising (2: 30 – 35):

reading said computer instructions in blocks (2: 33, discloses determining the location of target definitions for branch operations within the program, this would require the instruction to be read, inherently);

defining a set of target registers associated with each block for holding target addresses for the set branch instructions in that block (2:37 – 40);

defining as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state (4: 12 – 17); and

using said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses (5: 16 – 19, see " no other family that uses that target register has a target definition located in the loop).

Regarding claim 2, a method according to claim 1, which comprises the steps of:

allocating each set branch instruction to an initial node in a dominator tree (FIG. 15, see 1501 and also dom list and refer to fig, 1 and 2 for tree like structure and 2: 44 for dominator block) , said initial node being the node which contains the corresponding effect branch instruction (FIG. 15, 1502); and

migrating one or more said branch instruction to an ancestor node in the dominator tree (Fig 3, 302, shows *(migrating)* branching to ancestor node).

Regarding claim 3, a method according to claim 2, wherein, during said step of migrating said at least one set branch instruction, the live range of blocks is incrementally updated (8: 65 – 67).

Regarding claim 4, a method according to claim 3, wherein, during said step of migrating said at least one set branch instruction, the set of target registers holding target

addresses in a live state is simultaneously incrementally updated (12:30 – 40).

Regarding claim 5, a method according to claim 1, wherein the union of said set of target registers and said live range is taken to define target registers holding target addresses in a live state(14: 10 –20, and lines 60 – 67).

Regarding claim 6, Callahan anticipates a method of operating a computer system to compile a computer program from a sequence of computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch and a plurality of second, effect branch instructions which each implement a branch to the target address specified in the associated set branch instruction, the method comprising (2: 30 – 35):

executing a dominator tree constructor function in the computer system to read said computer instructions in blocks and to define a set of target registers associated with each block for holding target addresses for the set branch instructions in that block (4:15 – 25);

executing a lifetime tracking algorithm to define as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state, said lifetime tracking algorithm being operable to use said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses (7:25 – 33, see dominator list and keeping track of live ranges).

Regarding claim 7, a method according to claim 5, which comprises the step of executing a migration function which migrates at least one set branch instruction to an ancestor node in the dominator tree (Fig 3, 302, shows *(migrating)* branching to ancestor node).

Regarding claim 8, a method according to claim 6, wherein said lifetime tracking algorithm is operable to define said live range of blocks on an incremental basis as the at

least one set branch instruction is migrated (7:25 – 33, see dominator list and keeping track of live ranges).

Regarding claim 9, which discloses the computer program version of claim 1, see rationale as previously discussed above.

Regarding claim 10, which discloses the computer program version of claim 2, see rationale as previously discussed above.

Regarding claim 11, a compiler according to claim 9, which comprises a determiner for determining the effect of migrating said set branch instruction to each of a set of ancestor nodes in the dominator tree based on a performance cost parameter (12:30 – 40).

Response to Arguments

5. Applicant's arguments filed 12/28/04 have been fully considered but they are not persuasive. Applicant argues on page 5 of response, that Callahan doesn't disclose "prevent the target register being available for other uses".

Examiner believes that Callahan does in fact disclose this limitation. As claimed Applicant merely discloses using the live ranges to ensure the prevention of the target register being available for other uses. Applicant doesn't mention how this is being performed and hence is being read as being disclosed by Callahan's teachings. Examiner believes this limitation is taught by Callahan. Callahan discloses using target definitions in the preheaders associated with the live ranges to prevent the register from being available for others and restricted to only the family which it encompasses (5: 16 – 25). Examiner understands this to be equivalent to "using said set of target registers and said live ranges to ensure that target registers holding target addressed in a live state are not available for other uses". Regarding all other arguments in claims 2 – 11, Applicant simply rehashes the arguments that has been discussed above.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUAN DAM
SUPERVISORY PATENT EXAMINER

Ck.